(19) JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: **08083487 A**

(43) Date of publication of application: **26.03.96**

(51) Int. Cl **G11C 11/409**
**H01L 27/04**
**H01L 21/822**
**H01L 27/06**

(21) Application number: **06215658**

(22) Date of filing: **09.09.94**

(71) Applicant: **MITSUBISHI ELECTRIC CORP**

(72) Inventor: **ARIMOTO KAZUTAMI**
**TSUKIDE MASAKI**

# (54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

(57) Abstract:

PURPOSE: To prevent the increase of-access delay while reducing the current consumption at the time of standby cycles by setting the voltage level of a sub-power source voltage line in accordance with a reference voltage using a voltage setting circuit.

CONSTITUTION: When, at the time of stand-by cycles, the operation cycle regulating signals/ϕ, ϕ are at the H- and L-levels respectively, the p transistor(TR) Q1 and nTR Q2 are conducting, and the voltage of the sub-power source line 2 is higher than a reference voltage $V_{ref}$ 1 outputted by the reference voltage generator circuit 10, the voltage is set at $V_{ref}$ 1 by the differential amplifier of the voltage setting circuit. Similarly, the voltage of the sub-power source line 4 is set at a reference voltage $V_{ref}$ 2. Consequently, the pTR and nTR of the inverters $f_1$ to $f_3$ are controlled and the sub-threshold current is reduced, resulting in the decrease of current consumption at the time of standby cycles. Similarly at the time of operating cycles, the operating voltages immediately change from reference voltages, $V_{ref}$ 1 and $V_{ref}$ 2, to power source voltages, $V_{cc}$ and $V_{ss}$ respectively, preventing the increase of the access delay.